

Quad Sine-Wave Clock Buffer With LDO

Check for Samples: [CDC3S04](#)

FEATURES

- **1:4 Low-Jitter Clock Buffer**
- **Single-Ended Sine-Wave Clock Input and Outputs**
- **Ultralow Phase Noise and Standby Current**
- **Individual Clock Request Inputs for Each Output**
- **On-Chip Low-Dropout Output (LDO) for Low-Noise TCXO Supply**
- **Serial I²C Interface (Compatible With High-Speed Mode, 3.4 Mbit/s)**
- **1.8-V Device Power Supply**
- **Wide Temperature Range, –40°C to 85°C**
- **ESD Protection: 2 kV HBM, 750 V CDM, and 100 V MM**
- **Small 20-Pin Chip-Scale Package: 0.4-mm Pitch WCSP (1.6 mm × 2 mm)**

APPLICATIONS

- **Cellular Phones**
- **Smart Phones**
- **Mobile Handsets**
- **Portable Systems**
- **Wireless Modems Including GPS, WLAN, W-BT, D-TV, DVB-H, FM Radio, WiMAX, and System Clock**

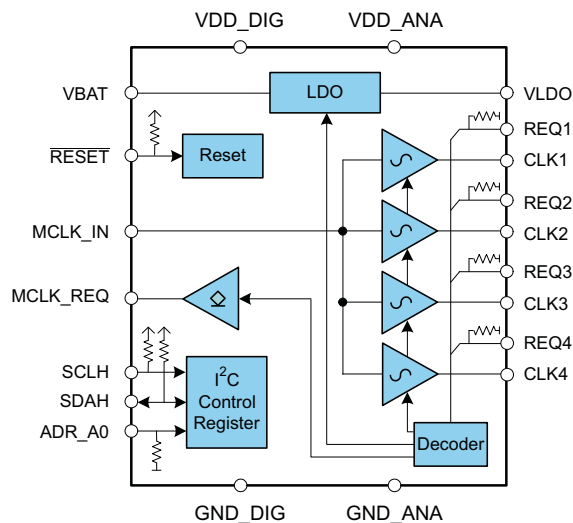
DESCRIPTION

The CDC3S04 is a four-channel low-power low-jitter sine-wave clock buffer. It can be used to buffer a single master clock to multiple peripherals. The four sine-wave outputs (CLK1–CLK4) are designed for minimal channel-to-channel skew and ultralow additive output jitter.

Each output has its own clock request inputs which enables the dedicated clock output. These clock requests are active-high (can also be changed to be active-low via I²C), and an output signal is generated that can be sent back to the master clock to request the clock (MCLK_REQ). MCLK_REQ is an open-source output and supports the wired-OR function (default mode). It needs an external pulldown resistor. MCLK_REQ can be changed to wired-AND or push-pull functionality via I²C.

The CDC3S04 also provides an I²C interface (Hs-mode) that can be used to enable or disable the outputs, select the polarity of the REQ inputs, and allow control of internal decoding.

The CDC3S04 features an on-chip high-performance LDO that accepts voltages from 2.3 V to 5.5 V and outputs a 1.8-V supply. This 1.8-V supply can be used to power an external 1.8-V TCXO. It can be enabled or disabled for power saving at the TCXO.


WCSP

	1	2	3	4
A	REQ2	CLK2	REQ1	CLK1
B	MCLK_IN	RESET	VDD_ANA	GND_ANA
C	REQ4	CLK4	REQ3	CLK3
D	VDD_DIG	GND_DIG	MCLK_REQ	ADR_A0
E	VLDO	VBAT	SDAH	SCLH

Top View
(Solder Ball Underneath)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

CDC3S04

SCAS883C –OCTOBER 2009–REVISED AUGUST 2012

www.ti.com


This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

A low signal at the **RESET** input switches the outputs CLK1 and CLK4 into the default state. In this configuration, CLK1 and CLK4 are ON (see [Table 1](#)); the remaining device function is not affected. Also, the **RESET** input provides a glitch filter which rejects spikes of typical 300 ns on the **RESET** line to preserve false reset. A complete device reset to the default condition can be initiated by a power-up cycle of V_{DD_DIG}.

The CDC3S04 operates from two 1.8-V supplies. There is a core supply (VDD_DIG/GND_DIG) for the core logic and a low-noise analog supply (VDD_ANA/GND_ANA) for the sine-wave outputs. The CDC3S04 is designed for sequence-less power up. Both supply voltages may be applied in any order.

The CDC3S04 is offered in a 0.4-mm pitch WCSP package (1.6 mm × 2 mm) and is optimized for low standby current (0.5 µA). It is characterized for operation from –40°C to 85°C.

DEVICE INFORMATION

PIN FUNCTIONS

NAME	BALL NO.	TYPE	FUNCTION
ADR_A0	D4	Input	Selectable address bit A0 of slave-address register; internal 500-kΩ pulldown resistor
CLK1	A4	Output	Clock output 1
CLK2	A2	Output	Clock output 2
CLK3	C4	Output	Clock output 3
CLK4	C2	Output	Clock output 4
GND_ANA	B4	Ground	Ground for sine-wave buffer
GND_DIG	D2	Ground	Ground for core logic
MCLK_IN	B1	Input	Master clock input
MCLK_REQ	D3	Output	Clock request to the master clock source; active-high; open-source output for wired-OR connection (default condition). Can be changed to push-pull output or wired-AND output via I ² C.
REQ1	A3	Input	Clock request from peripheral 1; internal 500-kΩ pulldown resistor
REQ2	A1	Input	Clock request from peripheral 2; internal 500-kΩ pulldown resistor
REQ3	C3	Input	Clock request from peripheral 3; internal 500-kΩ pulldown resistor
REQ4	C1	Input	Clock request from peripheral 4; internal 500-kΩ pulldown resistor
RESET	B2	Input	Peripheral reset signal provided by application processor. The signal is active-low and switches CLK1 and CLK4 outputs to ON (see Table 1). On-chip LDO is enabled. Internal 1-MΩ pullup resistor and 300-ns (typ) glitch filter.
SCLH	E4	Input	I ² C clock input – Hs-mode. Internal 1-MΩ pullup resistor
SDAH	E3	Input/output	I ² C data input/output – Hs-mode. Internal 1-MΩ pullup resistor
VBAT	E2	Power	Supply pin to internal LDO
VDD_ANA	B3	Power	1.8-V power supply for sine-wave buffer
VDD_DIG	D1	Power	1.8-V power supply for core logic. Power up of VDD_DIG resets the whole device to the default condition.
VLDO	E1	Output	1.8-V supply for external TCXO; LDO is enabled if RESET (default mode) or REQx is active. LDO is not enabled if only VBAT is on.

FUNCTION SELECTION TABLES

Table 1. Reset and Request (REQx) Conditions for Clock Outputs⁽¹⁾

RESET ⁽²⁾	PRIORITY BIT ⁽³⁾	CLK1	CLK2	CLK3	CLK4
0	0	On	Controlled by REQ2	Controlled by REQ3	On
	1		Controlled by REQ2INT	Controlled by REQ3INT	
1	0	Controlled by REQ1	Controlled by REQ2	Controlled by REQ3	Controlled by REQ4
	1	Controlled by REQ1INT	Controlled by REQ2INT	Controlled by REQ3INT	Controlled by REQ4INT

- (1) Shaded cells show the default setting after power up.
(2) RESET resets REQ1PRIO/REQ4PRIO and REQ1INT/REQ4INT bits to their default values (CLK1/4 is ON) but does not change the remaining internal SW bits. During RESET, any I²C operation is blocked until RESET is deactivated. A minimum pulse duration of 500 ns must be applied to activate RESET (the internal glitch-filter suppresses spikes of typical 300 ns).
(3) Priority bit defines if the external control pins (HW controlled) or the SW bits (SW controlled) have priority. It can be set in the configuration register, Byte 2, Bits 0–3.

Table 2. Request Signal Condition for Clock Outputs⁽¹⁾

REQ-Signals ⁽²⁾	REQx (REQ1/2/3/4)	CLKx (CLK1/2/3/4)	MCLK_REQ	LDO ⁽³⁾
Active-low	0	Clock	High	On
	1	Disabled to high	Low (if all REQx are high)	Off (if all REQx are high)
Active-high	0	Disabled to high ⁽⁴⁾	Low (if all REQx are low)	Off (if all REQx are low)
	1	Clock ⁽⁴⁾	High	On

- (1) Shaded cells show the default setting after power up.
(2) Polarity of REQ1, REQ2, REQ3, and REQ4 are register-configurable via I²C (see Table 3, Byte 0, Bits 0–3). Default setting is active-high.
(3) The LDO is controlled by an on-chip decoder, but can also be SW controlled (see Table 3, Byte 2, Bits 4–5).
(4) CLK1 and CLK4 are ON after device power up (default condition). CLK2 and CLK3 are controlled by external REQ2 and REQ3, respectively.

POWER GROUPS

NAME	DESCRIPTION
VBAT	Supply pin for LDO provided by main battery. LDO is not working if only VBAT is on.
VLDO	1.8-V low-drop output voltage for external TCXO. LDO is enabled if VBAT and VDD_DIG are on and REQx or RESET is active (see Table 2).
VDD_DIG	1.8-V power supply for core logic and I ² C logic. VDD_DIG must be supplied for correct device operation. Power up of VDD_DIG resets the whole device to the default condition.
VDD_ANA	1.8-V power supply for sine-wave buffers. For correct sine-wave buffer function, all three power supplies (VBAT, VDD_DIG and VDD_ANA) must be on. But, VDD_ANA can be switched on and off at any time. If off, the sine-wave outputs are switched to high-impedance.

POWER-UP SEQUENCE

The CDC3S04 is designed for sequence-less power up. VBAT, VDD_DIG, and VDD_ANA may be applied in any order. Recommended power-on sequence is VBAT first, followed by VDD_DIG and VDD_ANA. Recommended power-off sequence is in reverse order.

CDC3S04

SCAS883C –OCTOBER 2009–REVISED AUGUST 2012

www.ti.com

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		VALUE	UNIT
V _{DD_ANA} V _{DD_DIG}	Supply voltage range	–0.5 to 2.5	V
V _{BAT}	Battery supply voltage range	–0.5 to 6.5	V
V _I	Input voltage range ^{(2) (3)}	–0.5 to V _{DD} + 0.5	V
V _O	Output voltage range ^{(2) (3)}	–0.5 to V _{DD} + 0.5	V
V _{LDO}	Output voltage range	–0.5 to V _{BAT} + 0.5	V
	Input current (V _I < 0, V _I > V _{DD})	±20	mA
I _O	Continuous output current	±20	mA
I _{LDO}	Continuous output current	±20	mA
T _{stg}	Storage temperature range	–65 to 150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The input V_I and output V_O positive voltages are limited to the absolute maximum rating for V_{DD} = 2.5 V.

THERMAL CHARACTERISTICS for 20-pin WCSP (YFF) ⁽¹⁾

PARAMETER	AIRFLOW (lfm)	20-PIN WCSP	UNIT
T _{JA} Thermal resistance, junction-to-ambient	0	71	°C/W
	200	62	
	400	59	
T _{JC} Thermal resistance, junction-to- case	–	17.5	°C/W
T _{JB} Thermal resistance, junction-to-board	–	20.5	°C/W
T _J Maximum junction temperature	–	125	°C

- (1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
V _{DD_ANA} Device supply voltage	1.65	1.8	1.95	V
V _{DD_DIG} Device supply voltage	1.65	1.8	1.95	V
V _{IH}	0.65 V _{DD_DIG}			V
V _{IL}				V
V _{IS} Sine-wave input voltage – MCLK_IN; ac-coupled amplitude	0.5		1.2	V _{PP}
C _L Sine-wave output load ⁽¹⁾		10	30	pF
C _{OUT} LDO output capacitance (stabilize the internal control loop)	0.8	2.2		μF
T _A Operating free-air temperature	–40		85	°C

- (1) 10 pF is the typical load-driving capability. The drive capability can be optimized for 30 pF by the I²C register (Byte 3, Bits 7–4).

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OVERALL PARAMETER							
I _{DD_ANA}	Analog supply current ⁽¹⁾ (see Figure 8 through Figure 12)	V _{BAT} = 5.5 V; V _{DD_ANA} = 1.95 V; LDO is on; V _{IS} = 1 V _{PP} ; f _{MCLK_IN} = 38.4 MHz; R _L = 10 kΩ; C _L = 10 pF ⁽²⁾	Off (no REQ)		0.1	0.2	mA
			Per output		2	2.6	
I _{DD_DIG}	Digital supply current (see Figure 8 through Figure 12)	V _{BAT} = 5.5 V; V _{DD_DIG} = 1.95 V; V _{DD_ANA} = off; LDO = off; V _{IS} = 1 V _{PP} ; f _{MCLK_IN} = 38.4 MHz; C _L = 10 pF; R _L = 10 kΩ				0.1	mA
I _{SB}	Standby current	V _{BAT} = 5.5 V; V _{DD_DIG} /V _{DD_ANA} = 1.95 V; All outputs disabled (no input clock; LDO off; no REQ; RESET is inactive; I ² C is in idle mode); includes 1-MΩ pullup at I ² C and RESET			0.5	10	μA
f _{MCLK_IN}	Input frequency	Sine wave		0.01	38.4	52	MHz
V _{OH}	MCLK_REQ high-level output voltage	Wired-OR output; I _{OH} = −2 mA; V _{DD_DIG} = 1.65 V (See Figure 3.)		V _{DD_DIG} − 0.45			V
		Push-pull output; V _{DD_DIG} = 1.65 V, I _{OH} = −2 mA		V _{DD_DIG} − 0.45			
V _{OL}	MCLK_REQ low-level output voltage	Wired-AND output; I _{OL} = 2 mA V _{DD_DIG} = 1.65 V		0.45			V
		Push-pull output; V _{DD_DIG} = 1.65 V, I _{OL} = 2 mA		0.45			
V _{IK}	LVC MOS input voltage	V _{DD_DIG} = 1.65 V; I _I = −18 mA				−1.2	V
I _{IH}	Input current ADR_A0, REQx (500-kΩ pulldown)	V _I = V _{DD_DIG} ; V _{DD_DIG} = 1.95 V				6	μA
	Input current RESET (1-MΩ pullup)					2	
I _{IL}	Input current ADR_A0, REQx (500-kΩ pulldown)	V _I = 0 V; V _{DD_DIG} = 1.95 V				−2	μA
	Input current RESET (1-MΩ pullup)					−3	
C _I	Input capacitance ADR_A0, REQx, RESET	V _I = 0 V or V _{DD_DIG}			3		pF
SDAH/SCLH PARAMETER (Hs-Mode)							
V _{IK}	SCLH/SDAH input clamp voltage	V _{DD_DIG} = 1.65 V; I _I = −18 mA				−1.2	V
I _I	SCLH/SDAH input current	0.1 V _{DD_DIG} < V _I < 0.9 V _{DD_DIG}				10	μA
V _{IH}	SDA/SCL input high voltage			0.7 V _{DD_DIG}			V
V _{IL}	SDAH/SCLH input low voltage			0.3 V _{DD_DIG}			V
V _{hys}	Hysteresis of Schmitt-trigger inputs			0.1 V _{DD_DIG}			V
V _{OL}	SDAH low-level output voltage	I _{OL} = 3 mA, V _{DD_DIG} = 1.65 V		0.2 V _{DD_DIG}			V
C _I	SCLH input capacitance	V _I = 0 V or V _I = V _{DD_DIG} ⁽³⁾			3	5	pF
	SDAH input capacitance	V _I = 0 V or V _I = V _{DD_DIG} ⁽³⁾			8	10	

(1) The total current consumption when no output is active is calculated by $I_{DD_ANA}(\text{off}) + I_{DD_DIG}$.

(2) For $C_L = 30\text{ pF}$, the typical current for one output is 2.2 mA (see Figure 8).

(3) The I^2C standard specifies a maximum C_I of 10 pF.

CDC3S04

SCAS883C –OCTOBER 2009–REVISED AUGUST 2012

www.ti.com

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SINE-WAVE PARAMETER (MCLK_IN is sine-wave signal, C _L = 10 pF)							
f _{OUT}	Output frequency			52			MHz
V _{OS}	Output gain level (see Figure 17)	MCLK_IN-to-CLKx; 10 kΩ, 10 pF; ac-coupled;	0.5 ≤ V _{IS} ≤ 1.2 V _{PP}	−1	−0.3	0	dB
	Output voltage	f _{MCLK_IN} > 1 MHz	V _{IS} = 0.5 V _{PP}	445	490	500	mV _{PP}
t _{jittadd(rms)}	Additive rms jitter ⁽⁴⁾	10 Hz to 10 MHz; f _{OUT} = 38.4 MHz		0.3			pS _{RMS}
		10 kHz to 10 MHz; f _{OUT} = 38.4 MHz		0.1			
p _n _{add}	Additive phase noise at f _{OUT} = 38.4 MHz ⁽⁵⁾	At offset = 1 kHz		−142			dBc/Hz
		At offset = 10 kHz		−152			
		At offset = 100 kHz		−157			
R _{IN}	Input resistance	At dc level		12	15		kΩ
C _{IN}	Input capacitance	f _{MCLK_IN} = 38.4 MHz			5	7	pF
ELECTRICAL CHARACTERISTIC of LDO (C _{OUT} = 0.8 to 2.7 μF) ⁽⁶⁾							
V _{BAT}	Input voltage range			2.3		5.5	V
V _{LDO}	LDO output voltage ⁽⁷⁾	2.3 V < V _{BAT} < 5.5 V, I _{LOAD} = 5 mA		1.72	1.8	1.9	V
ΔV _{LDO}	Maximum line regulation	2.3 V < V _{BAT} ≤ 5.5 V, I _{LOAD} = 5 mA		0.5%			
	Maximum load regulation	0 < I _{LOAD} < 5 mA, V _{BAT} = 2.3 V or 5.5 V; T _J = 25°C		0.5%			
I _{LOAD}	Load current	C _{OUT} = 0.8 μF to 2.7 μF		0	5		mA
I _{LCL}	LDO output current limit	V _{LDO} = 0.9 × V _{LDO(TYP)}		10		60	mA
I _{LGND}	LDO ground pin current ⁽⁸⁾	V _{BAT} = 3.6 V; 0 < I _{LOAD} < 5 mA			50	150	μA
I _{LSHDN}	LDO shutdown current	2.3 V < V _{BAT} < 5.5 V				0.2	μA
PSRR	Power-supply rejection ratio (ripple rejection) (see Figure 20)	V _{BAT} = 2.3 V (for min) V _{BAT} = 2.5 V (for typ) V _{LDO} = 1.8 V I _{LOAD} = 5 mA V _{ripple} = 0.1 V _{pp}	100 Hz	60	68	dB	
			1 kHz	55	62		
			10 kHz	45	52		
			100 kHz	33	40		
			1 MHz	37	46		
			10 MHz	60	67		
V _N	Output noise voltage (see Figure 21)	BW = 10 Hz to 100 kHz; V _{LDO} = 1.8 V; I _{LOAD} = 5 mA		30			μV _{RMS}

(4) Additive rms jitter is the integrated rms jitter that the device adds to the signal chain. It is calculated by

$$t_{jitteradd(rms)} = \sqrt{(t_{jitterout(rms)})^2 - (t_{jitterin(rms)})^2}$$

. Specified with the supply ripple noise of 30 μV(rms) from 10 Hz to 100 kHz.

(5) Additive phase noise is the amount of phase noise that the device adds to the signal chain. It is calculated by

$$L_{add} (dB) = 10 \log (10^{0.1 L_{out}} - 10^{0.1 L_{in}})$$

(6) Minimum C_{OUT} should be 100 nF to allow for stable LDO operation.

(7) LDO output voltage includes maximum line and load regulation.

(8) LDO ground pin current does not change over V_{BAT}.

TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted) $V_{LDO} = 1.8\text{ V}$; $C_L = 10\text{ pF}$; $R_L = 10\text{ k}\Omega$

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
TIMING PARAMETER						
t_{PD}	Propagation delay time	MCLK_IN-to-CLKx; $f_{MCLK_IN} = 38.4\text{ MHz}$			3	ns
t_{LH}	Propagation delay time, low-to-high	REQx-to-MCLK_REQ (wired-OR, $C_L = 15\text{ pF}$, $R_L = 10\text{ k}\Omega$);			15	ns
t_{CLK} ⁽²⁾	CLKx on-time – REQ-to-CLKx	$f_{MCLK_IN} = 38.4\text{ MHz}$; V_{DD_ANA} is on; $V_{IS} = 1\text{ V}$; $V_{OS} = -1\text{ dB}$ (see Figure 5 and Figure 6)		0.3	0.4	μs
	CLKx on-time – RESET-to-CLKx ⁽³⁾			0.6	0.8	μs
	CLKx off-time – REQ-to-CLKx				25	ns
	CLKx on-time – V_{DD_ANA} to-CLKx	$f_{MCLK_IN} = 38.4\text{ MHz}$; $V_{IS} = 1\text{ V}$; $V_{OS} = -1\text{ dB}$; measurement starts when V_{DD_ANA} is 90% of 1.7 V (see Figure 7)		20	50	μs
t_{SP}	Pulse duration of spikes that must be suppressed by the input filter for RESET ⁽³⁾				100	ns
$t_{sk(0)}$	Output skew ⁽⁴⁾	$f_{MCLK_IN} = 38.4\text{ MHz}$; CLK1-to-CLK4		25	50	ps
t_{LDO}	LDO on-time ⁽⁵⁾ – REQ-to-LDO; – RESET-to-LDO	$V_{LDO} = 1.7\text{ V}$, $I_{LDO} = 5\text{ mA}$, $2.3\text{ V} < V_{BAT} < 5.5\text{ V}$; $C_{OUT} = 2.7\text{ }\mu\text{F}$		100	300	μs

(1) All typical values are at nominal V_{DD_ANA} and V_{DD_DIG} .

(2) CLK on-time is measured with valid input signal ($V_{IS} = 1\text{ Vpp}$). In case a TXCO is used, the LDO and TCXO are already on.

(3) Pulses above 500 ns are interpreted as a valid reset signal. Total time from RESET-to-CLKx is the sum of $t_{SP} + t_{CLK_RESET}$.

(4) Output skew is calculated as the greater of the difference between the fastest and the slowest t_{PLH} or the difference between the fastest and the slowest t_{PHL} .

(5) LDO off-time depends on the discharge time of the R-C components (see [Figure 4](#)).

PARAMETER		MIN	MAX	UNIT
SDAH/SCLH TIMING REQUIREMENTS, Hs-Mode ($C_{BUS} = 100\text{ pF}$ for each I ² C line; see Figure 24 and Figure 25)				
f_{SCLH}	SCLH clock frequency	0	3.4	MHz
$t_{su(START)}$	START setup time (SCLH high before SDAH low)	160		ns
$t_{h(START)}$	START hold time (SCLH low after SDAH low)	160		ns
t_{LOW}	Low period of the SCLH clock	160		ns
t_{HIGH}	High period of the SCLH clock	60		ns
$t_{h(SDAH)}$	SDAH hold time (SDAH valid after SCLH low)	0 ⁽¹⁾	70	ns
$t_{su(SDAH)}$	SDAH setup time	10		ns
t_r	SCLH rise time	10	40	ns
	SDAH rise time	10	80	
t_f	SCLH fall time	10	40	ns
	SDAH fall time	10	80	
$t_{su(STOP)}$	STOP setup time	160		ns
t_{SP}	Pulse duration of spikes that must be suppressed by the input filter for SDAH and SCLH	0	10	ns

(1) A device must internally provide a data hold time to bridge the undefined period between V_{IH} and V_{IL} of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time.

PARAMETER MEASUREMENT INFORMATION

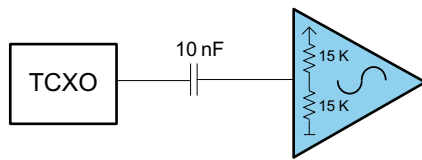


Figure 1. Input Circuit

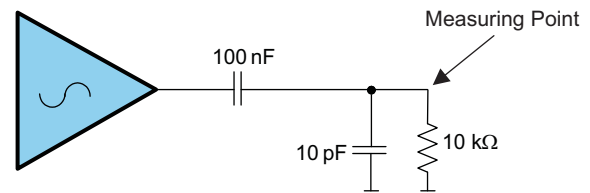


Figure 2. Output Circuit

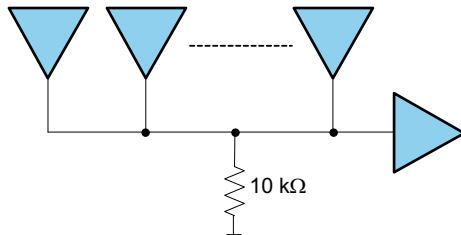
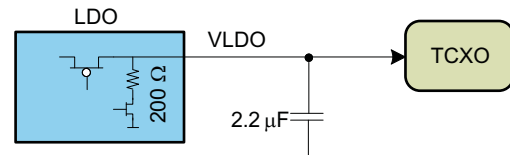


Figure 3. Wired OR



i.e. time constant(RxC) is $440\ \mu s$ for 63% discharge.

Figure 4. LDO Output Circuit

TYPICAL CHARACTERISTICS

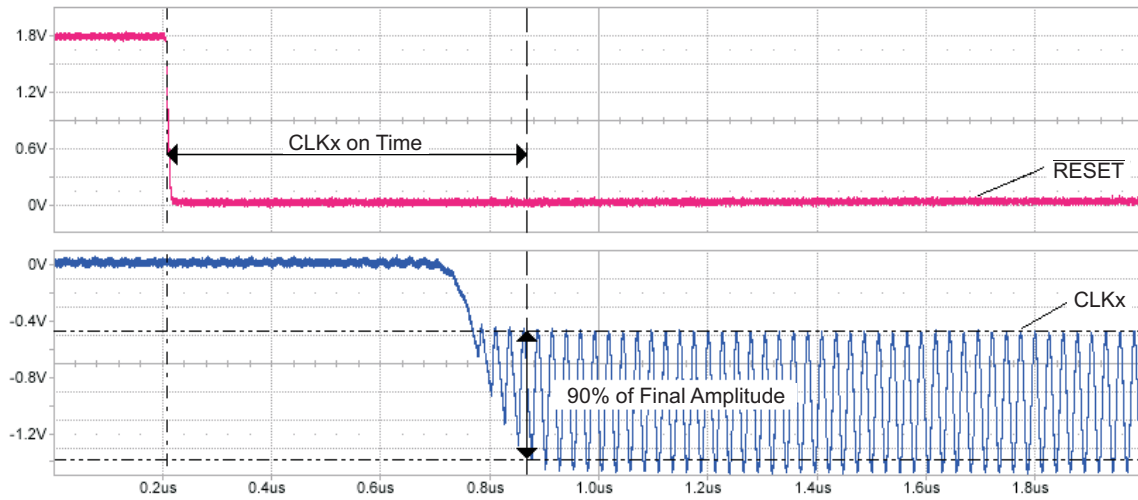


Figure 5. CLKx On-Time From $\overline{\text{RESET}}$ Off-to-On

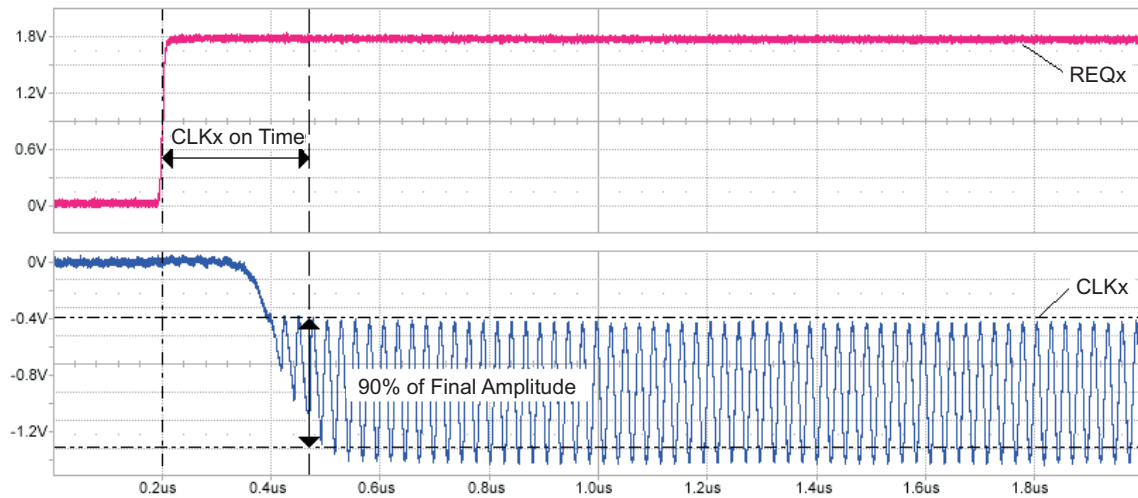


Figure 6. CLKx On-Time From REQ Off-to-On

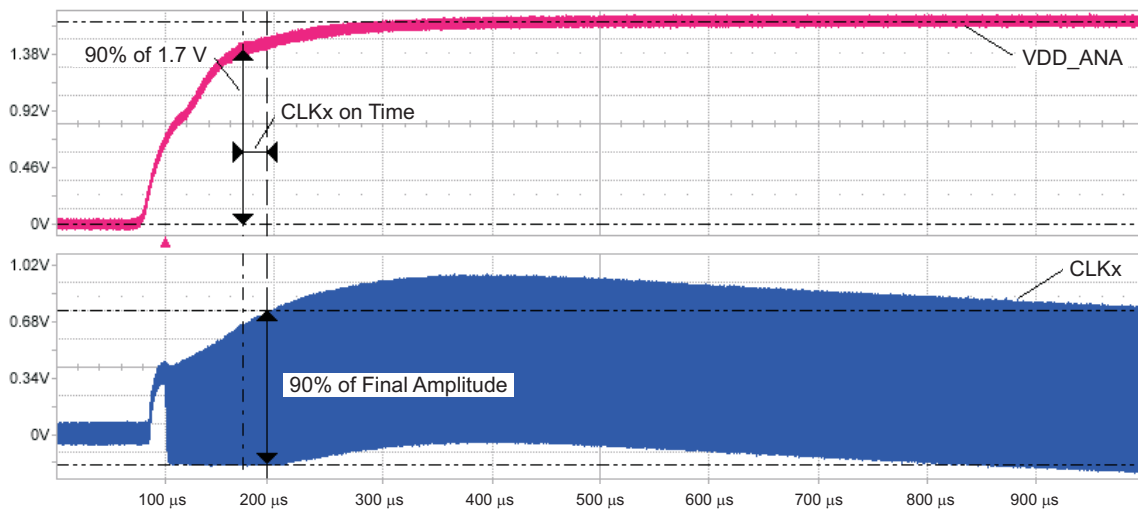


Figure 7. CLKx On-Time From $V_{\text{DD_ANA}}$ Off-to-On

TYPICAL CHARACTERISTICS (continued)

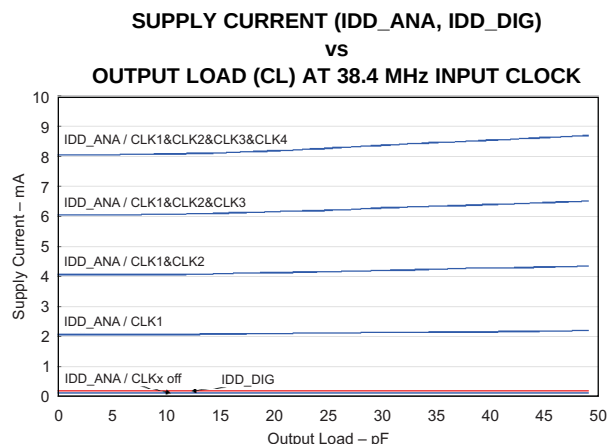


Figure 8.

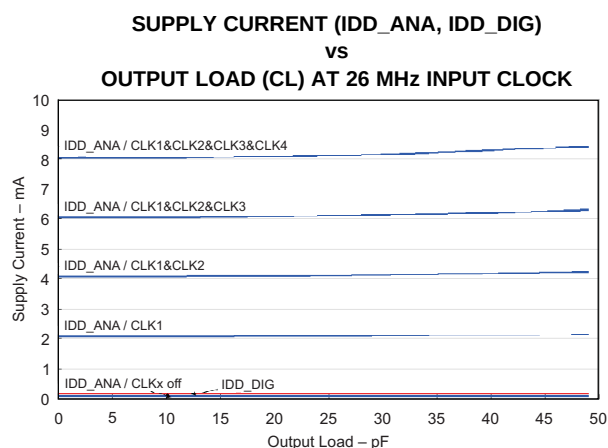


Figure 9.

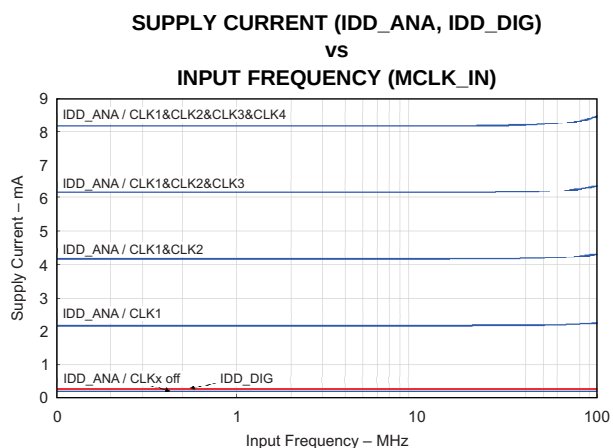


Figure 10.

TYPICAL CHARACTERISTICS (continued) **SUPPLY CURRENT (IDD_ANA, IDD_DIG)** **vs**

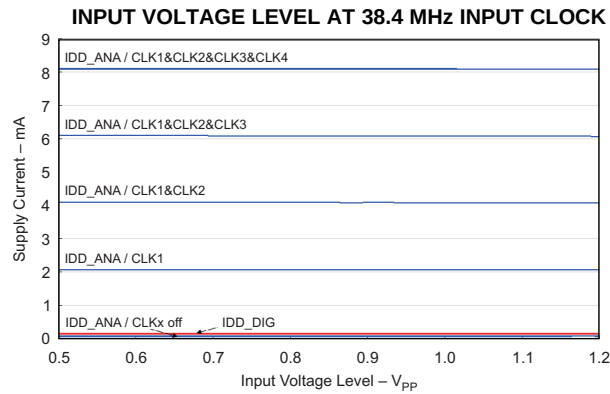


Figure 11.

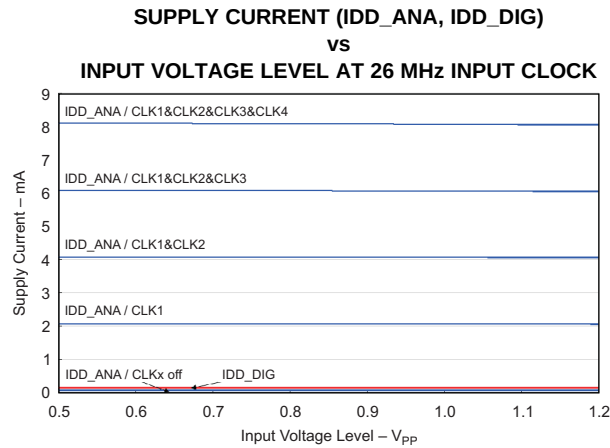


Figure 12.

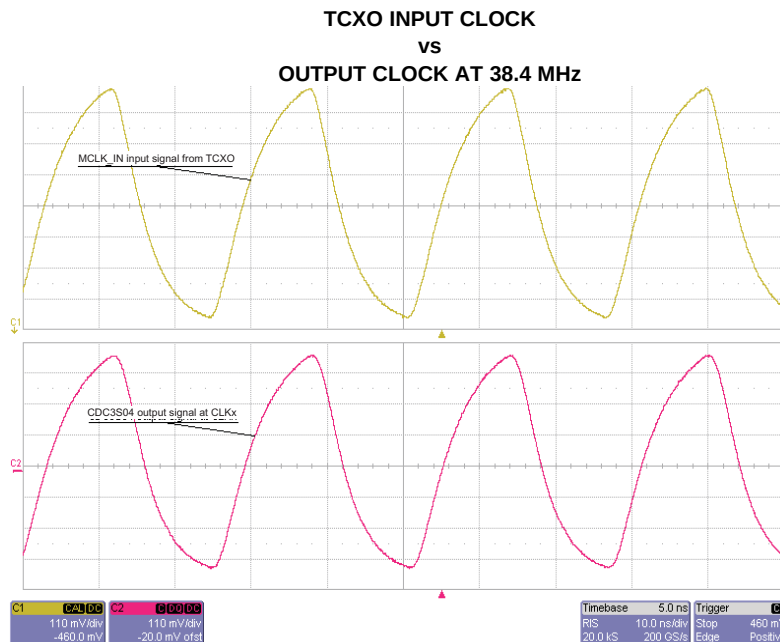


Figure 13.

TYPICAL CHARACTERISTICS (continued)

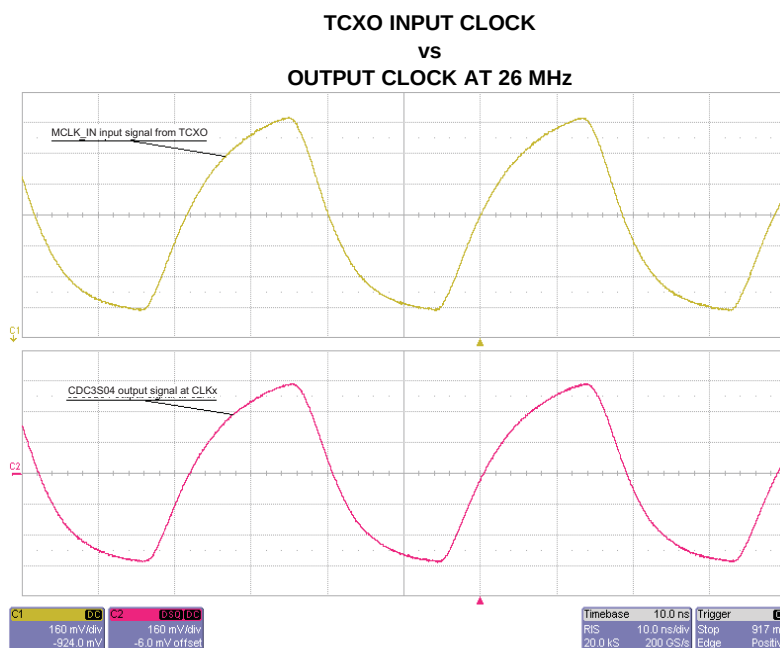


Figure 14.

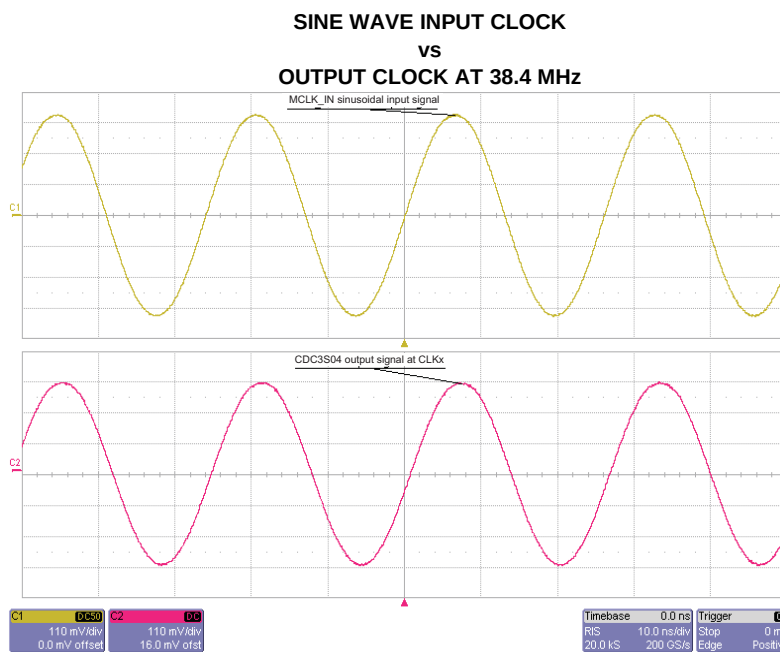


Figure 15.

TYPICAL CHARACTERISTICS (continued)

SINE WAVE INPUT CLOCK

vs

OUTPUT CLOCK AT 26 MHz

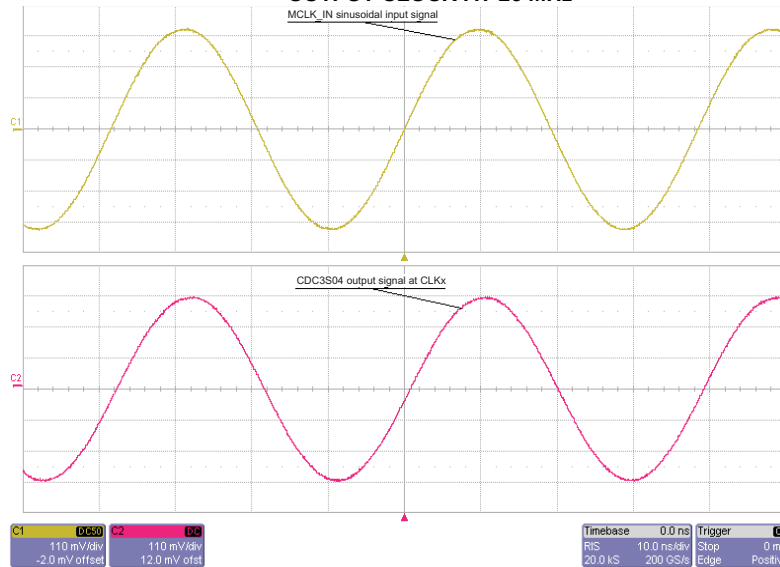


Figure 16.

OUTPUT GAIN

vs

INPUT FREQUENCY (MCLK_IN)

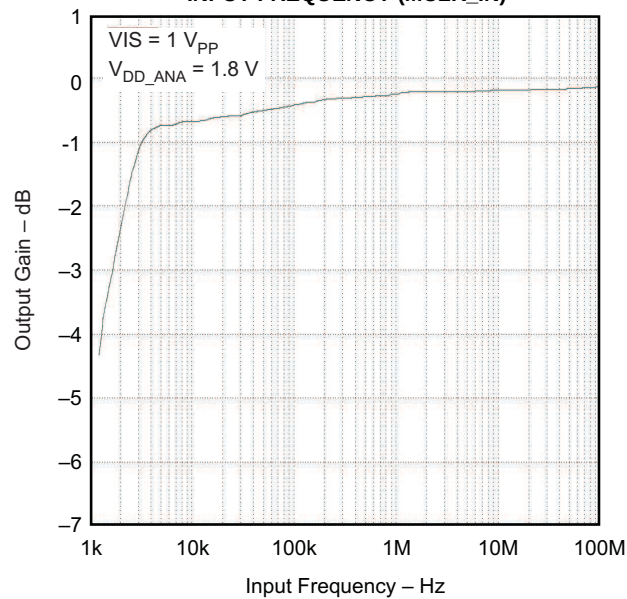


Figure 17.

TYPICAL CHARACTERISTICS (continued)

INPUT
vs
OUTPUT PHASE-NOISE PERFORMANCE WITH 38.4-MHz TCXO

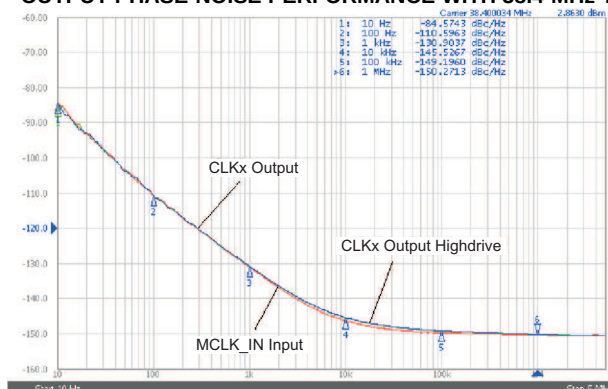


Figure 18.

INPUT
vs
OUTPUT PHASE-NOISE PERFORMANCE WITH 26-MHz TCXO

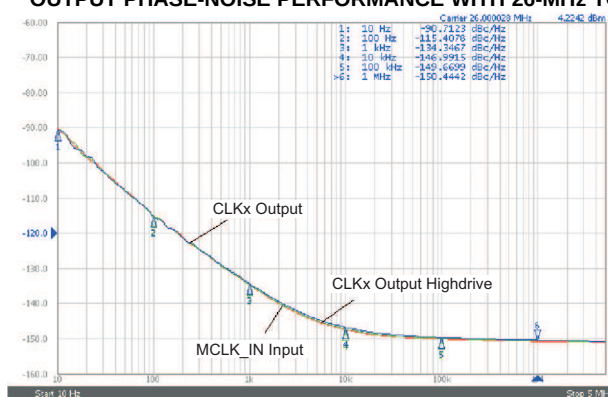


Figure 19.

LDO POWER SUPPLY REJECTION

vs
FREQUENCY (PSRR)

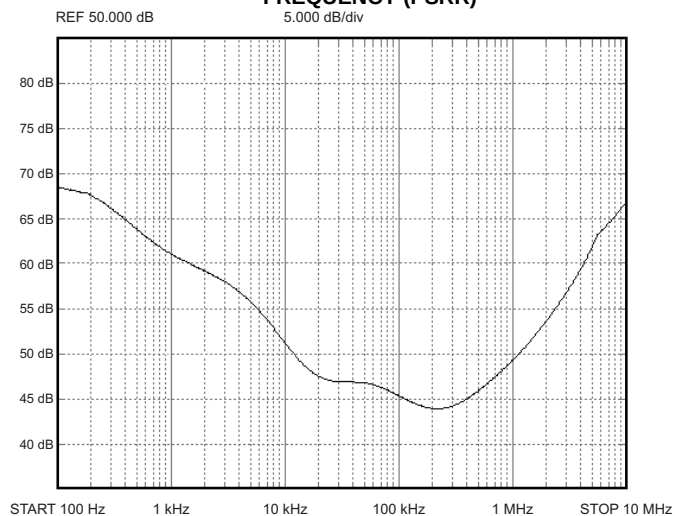


Figure 20.

TYPICAL CHARACTERISTICS (continued)

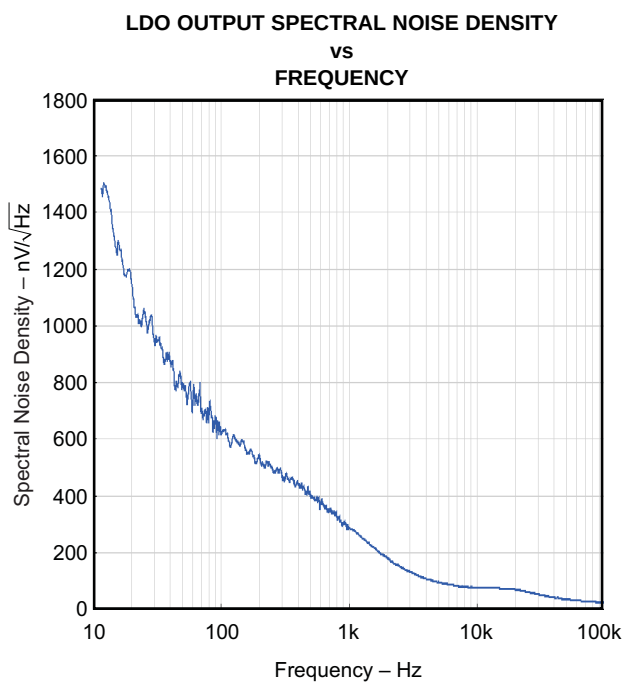


Figure 21.

DETAILED DESCRIPTION

SDAH/SCLH SERIAL INTERFACE (Hs-Mode)

This section describes the SDAH/SCLH interface of the CDC3S04 device. The CDC3S04 operates as a slave device of the two-wire serial SDAH/SCLH bus, compatible with the popular I²C specification (UM10204-I²C-bus specification and user manual Rev. 03–19 June 2007). It operates in the high-speed mode (up to 3.4 Mbit/s) and supports 7-bit addressing. The CDC3S04 is fully downward compatible with fast- and standard-mode (F/S) devices for bidirectional communication in a mixed-speed bus system.

Data Protocol

The device supports byte-write and byte-read operations only. There is no block-write or block-read operation supported; therefore, no command code byte is needed.

When a byte has been sent, it is written into the internal register and is immediately effective.

Slave Receiver Address (7 bits)

Device	A6	A5	A4	A3	A2	A1	A0 ⁽¹⁾	R/ $\overline{W}$
CDC3S04	1	1	0	1	1	0	0	1/0

(1) Address bit A0 is selectable by the ADR_A0 input (pin D1). This allows addressing of two devices connected to the same I²C bus. The default value is 0, set by an internal pulldown resistor.

Byte-Write Programming Sequence

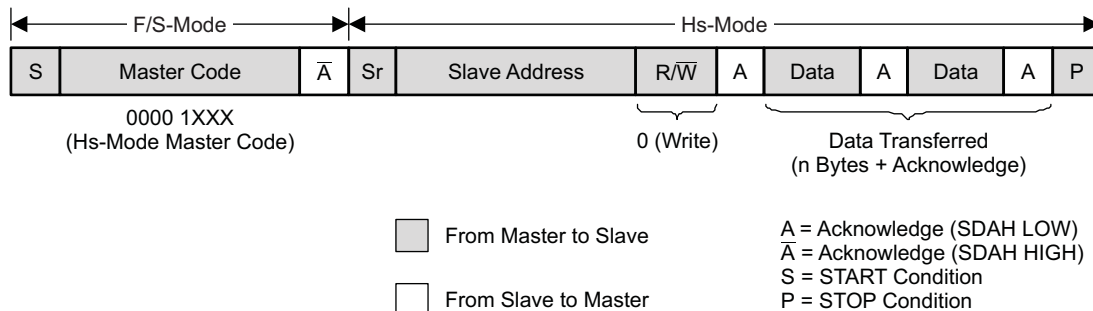


Figure 22. Byte-Write Protocol

Byte-Read Programming Sequence

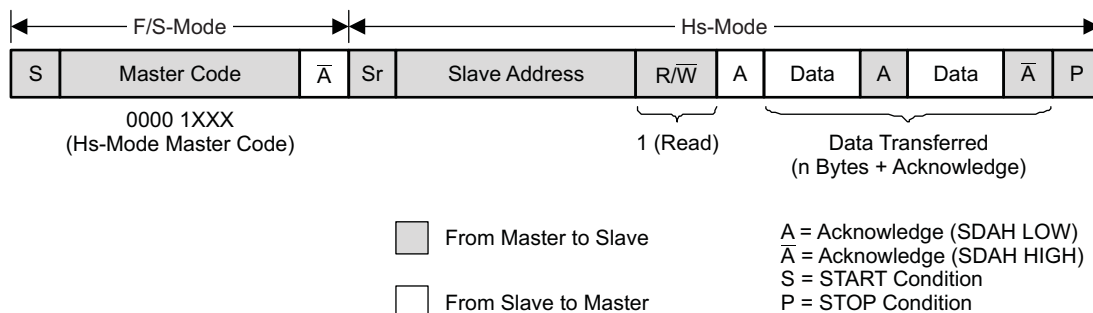
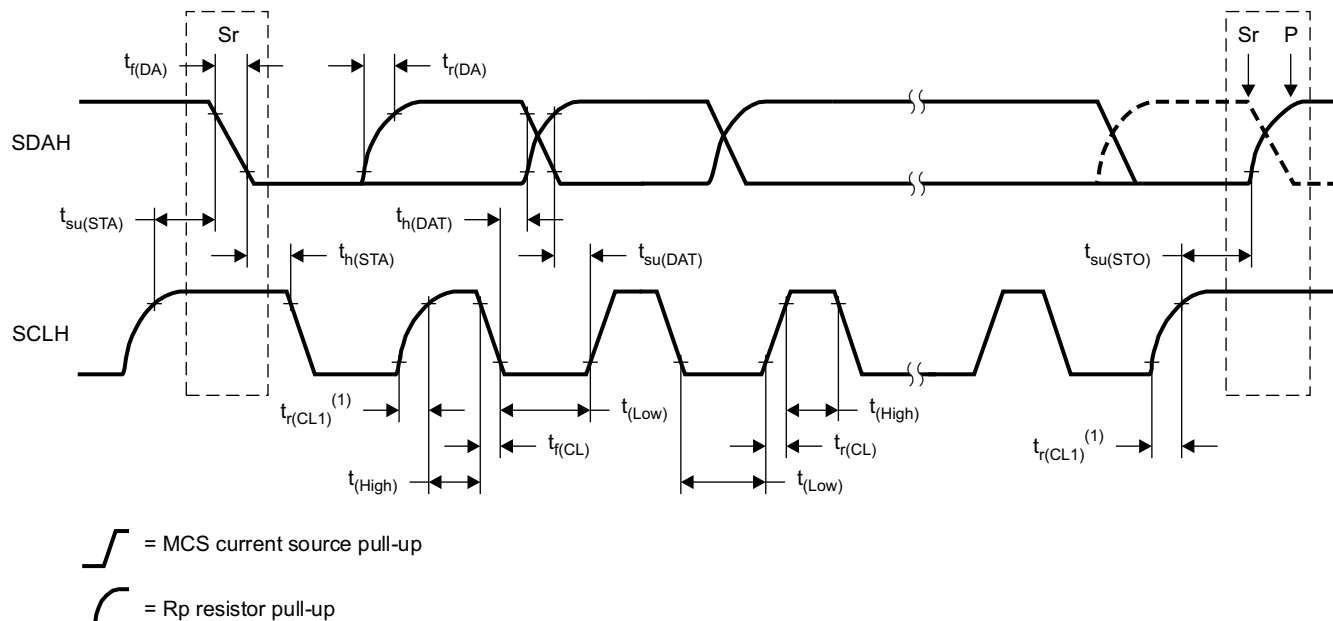


Figure 23. Byte-Read Protocol



T0451-01

(1) First rising edge of the SCLH signal after Sr and after each acknowledge bit.

Figure 24. Definition of Timing for a Complete Hs-Mode Transfer

The following diagram shows how the CDC3S04 clock buffer is connected to the SDAH/SCLH serial interface bus. Multiple devices can be connected to the bus, but the speed may need to be reduced (3.4 MHz is the maximum) if many devices are connected.

Note that the pullup resistors (R_p) depend on the supply voltage, bus capacitance, and number of connected devices. For more details, see the I²C bus specification.

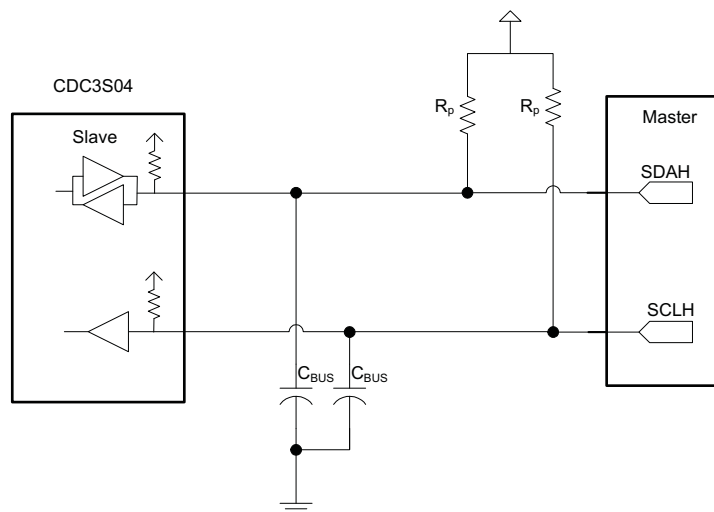


Figure 25. SDAH/SCLH Hardware Interface

SDAH/SCLH Configuration Registers

The output stages are user configurable. [Table 3](#) explains the programmable functions of the CDC3S04.

CDC3S04

SCAS883C –OCTOBER 2009–REVISED AUGUST 2012

www.ti.com
Table 3. Configuration Register (Shaded Cells Marks Power-Up/Default Setting)

Offset	BIT ⁽¹⁾	Acronym	Default ⁽²⁾	RESET ⁽³⁾	Description	0	1	Type
00h	7	REQ4INT	1b	1b	CLK4 off/on ⁽⁴⁾	Off	On	R/W
	6	REQ3INT	0b	–	CLK3 off/on ⁽⁴⁾	Off	On	
	5	REQ2INT	0b	–	CLK2 off/on ⁽⁴⁾	Off	On	
	4	REQ1INT	1b	1b	CLK1 off/on ⁽⁴⁾	Off	On	
	3	REQ4POL	1b	–	Selects polarity of REQ4	Active-low	Active-high	
	2	REQ3POL	1b	–	Selects polarity of REQ3	Active-low	Active-high	
	1	REQ2POL	1b	–	Selects polarity of REQ2	Active-low	Active-high	
	0	REQ1POL	1b	–	Selects polarity of REQ1	Active-low	Active-high	
01h	7	MREQ4	1b	–	Defines if REQ4 is used to decode MCLK_REQ	Not used for decoding	Used for decoding	R/W
	6	MREQ3	1b	–	Defines if REQ3 is used to decode MCLK_REQ			
	5	MREQ2	1b	–	Defines if REQ2 is used to decode MCLK_REQ			
	4	MREQ1	1b	–	Defines if REQ1 is used to decode MCLK_REQ			
	3	MCLKOUT1	00b	–	Selects MCLK_REQ output type 00 = wired-OR (default setting) 01 = wired-AND 1x = push-pull			
	2	MCLKOUT0						
	0–1	–	00b	–	Reserved			
02h	7	MREQCTRL1	00b	–	MCLK_REQ generation (see Figure 27) 0x = decoder controlled (default setting) 10 = low 11 = high			R/W
	6	MREQCTRL0						
	5	LDOEN1	00b	–	Switches LDO on or off: 00 = LDO is on (default setting) 01 = LDO is off 1x = decoder controlled (see Figure 27)			
	4	LDOEN0						
	3	REQ4PRIO	1b	1b	Defines external vs internal REQ4 priority	REQ4	REQ4INT	
	2	REQ3PRIO	0b	–	Defines external vs internal REQ3 priority	REQ3	REQ3INT	
	1	REQ2PRIO	0b	–	Defines external vs internal REQ2 priority	REQ2	REQ2INT	
	0	REQ1PRIO	1b	1b	Defines external vs internal REQ1 priority	REQ1	REQ1INT	
03h	7	HIGHDRIVE4	0b	–	Enables high-drive capability CLK4	Typical	High	R/W
	6	HIGHDRIVE3	0b	–	Enables high-drive capability CLK3	Typical	High	
	5	HIGHDRIVE2	0b	–	Enables high-drive capability CLK2	Typical	High	
	4	HIGHDRIVE1	0b	–	Enables high-drive capability CLK1	Typical	High	
	0–3	–	0b	–	Reserved			
04h–Bh ⁽⁵⁾		–		–	Reserved			R/W

- (1) All data is transferred with the MSB first.
- (2) A device reset to default condition is initiated by a V_{DD_DIG} power-up sequence.
- (3) "–" means that dedicated bits do not change at RESET.
- (4) Inactive as long as the REQxPRIO bit is low, external REQx pins are valid (see [Figure 26](#))
- (5) Writing data beyond 03h may affect device function.

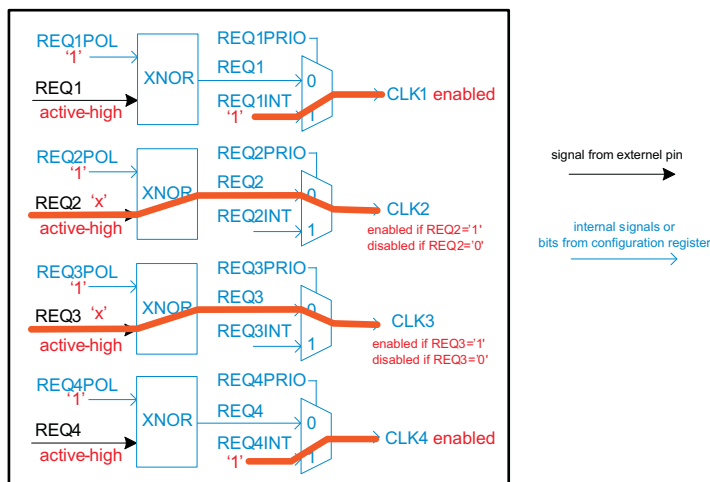


Figure 26. Clock Output Enable Signal
(Shaded Line Marks Power-Up/Default Setting)

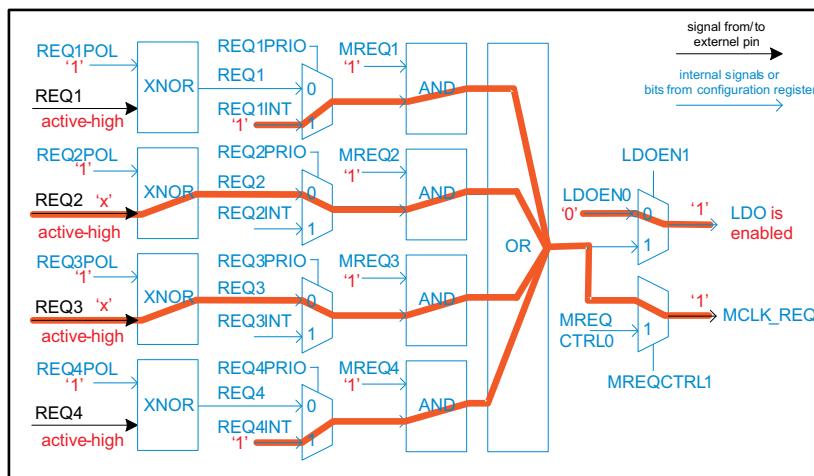


Figure 27. Decoding Scheme for MCLK_REQ and LDOEN
(Shaded Line Marks Power-Up/Default Setting)

APPLICATION INFORMATION

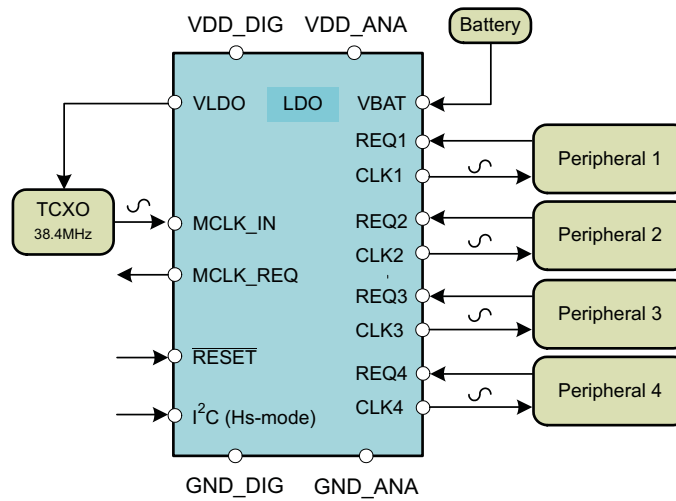


Figure 28. Clock Distribution Scheme

REVISION HISTORY

Changes from Original (October 2009) to Revision A	Page
- Changed the format on page 1 (moved 2 paragraphs from page 2 to page 1) - Changed the X axis from 0.1us to 100us....900us - Changed Offset 00h Bit 4 Default value from 0h to 1b	1 9 18
Changes from Revision A (July 2010) to Revision B	Page
Changed Table 3 "Offset" values listed in "Default" and "$\overline{\text{RESET}}$" columns from "h" to "b".	18
Changes from Revision B (May 2011) to Revision C	Page
- Changed from Rev B, 2011 to Rev C, 2012 - Changed the 8th Feature item from –30°C to –40°C - Changed in the last paragraph of description from –30°C to –40°C - Changed in the ROC table last row, from –30°C to –40°C	1 1 2 4

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CDC3S04YFFR	ACTIVE	DSBGA	YFF	20	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

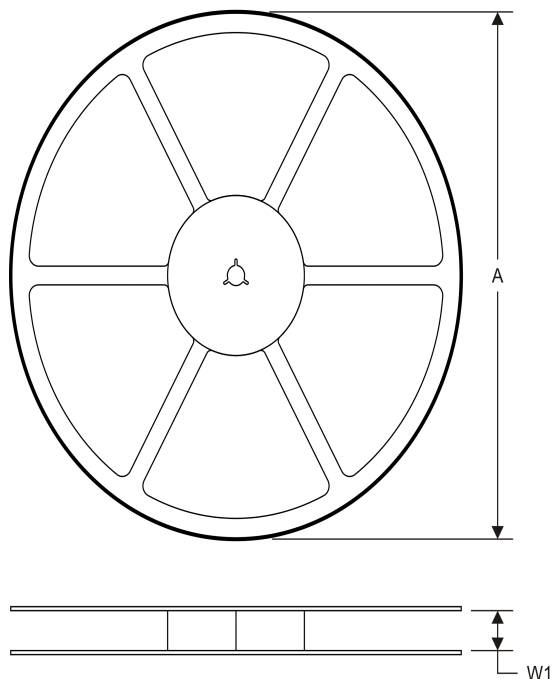
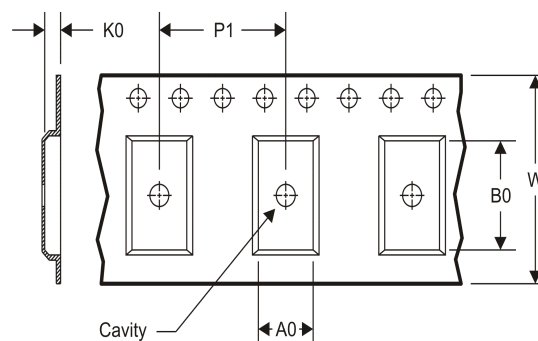
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


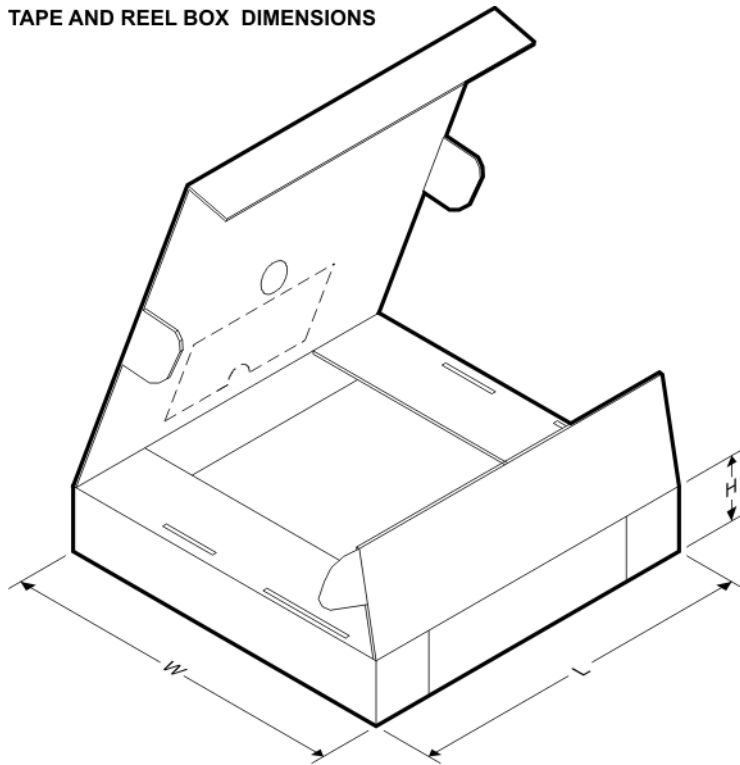
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC3S04YFFR	DSBGA	YFF	20	3000	180.0	8.4	1.63	2.08	0.69	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC3S04YFFR	DSBGA	YFF	20	3000	210.0	185.0	35.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com